

Claims

What is claimed is:

- 1 1. A decoder, comprising:  
 2 a feedback equalizer capable of receiving a modulated signal, the modulated signal  
 3 including a symbol defined by a first number of chips; and  
 4 a subsymbol processor coupled to said feedback equalizer to generate a subsymbol  
 5 waveform upon receipt of a second number of chips of the symbol and provide the  
 6 subsymbol waveform to the feedback equalizer, the second number being less than the first  
 7 number, said feedback equalizer to equalize the modulated signal using the subsymbol  
 8 waveform.
- 1 2. The decoder of Claim 1, wherein the subsymbol waveform includes a third number  
 2 of chips, the third number being less than or equal to the second number.
- 1 3. The decoder of Claim 1, said feedback equalizer comprising:  
 2 a hard decision unit coupled to said equalizer for determining hard decision  
 3 information associated with the modulated signal ; and  
 4 a feedback filter coupled to said hard decision unit and said symbol processor to  
 5 selectively equalize the modulated signal using one of the hard decision information and the  
 6 subsymbol waveform.
- 1 4. The decoder of Claim 1, wherein the symbol processor comprises:  
 2 a demodulation unit coupled said feedback equalizer and comprising subsymbol  
 3 decoding processing logic capable of generating decoded subsymbol information upon  
 4 perceiving the second number of chips of the symbol; and  
 5 a remodulation unit coupled to said demodulation unit and said feedback equalizer,  
 6 said remodulation unit generating a subsymbol waveform corresponding to the decoded  
 7 subsymbol information.
- 1 5. The decoder of Claim 4, wherein said demodulation unit further comprises a symbol  
 2 correlator coupled to said decoding processing logic to correlate the perceived second  
 3 number of chips against a subset of valid candidate symbols to obtain a best match

4 candidate, said decoding processing logic generating the decoded subsymbol information  
5 based on the best match candidate.

1 6. The decoder of Claim 4, wherein said demodulation unit further comprises decision  
2 processing logic capable of deciding the symbol upon receipt of the first number of chips  
3 defining the symbol.

1 7. The decoder of Claim 6, wherein said decision processing logic comprises first and  
2 second demodulation pathways capable of deciding the symbol by at least one of first and  
3 second distinct modulation modes.

1 8. The decoder of Claim 7, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

1 9. The decoder of Claim 1, wherein the symbol is modulated in accordance with one of  
2 Barker spreading and complementary code keying (CCK) compliant with IEEE Standard  
3 802.11b (1999).

1 10. A feedback equalizer comprising:  
2 a summing unit having an output and first input for receiving a modulated signal,  
3 the modulated signal including a symbol defined by a first number of chips;  
4 a subsymbol processor coupled to said output of said summing unit, said symbol  
5 processor capable of generating a subsymbol waveform upon receipt of a second number  
6 of chips of the symbol, the second number being less than the first number; and  
7 a feedback filter coupled to a second input of said summing unit and said symbol  
8 processing unit to selectively filter the subsymbol waveform from said modulated signal.

1 11. The equalizer of Claim 10, wherein the subsymbol waveform includes a third  
2 number of chips, the third number being less than or equal to the second number.

1 12. The equalizer of Claim 10, further comprising:  
2 a hard decision unit coupled to the output of said summing unit for determining hard  
3 decision information associated with the modulated signal ; and

4 a feedback filter coupled to said hard decision unit and said subsymbol processor to  
5 selectively equalize the modulated signal using one of the hard decision information and the  
6 subsymbol waveform.

1 13. The equalizer of Claim 10, wherein the symbol processor comprises:

2 a demodulation unit coupled said summing unit and comprising subsymbol decoding  
3 processing logic capable of generating decoded subsymbol information upon perceiving  
4 the second number of chips of the symbol; and

5 a remodulation unit coupled to said demodulation unit and said feedback filter, said  
6 remodulation unit generating a subsymbol waveform corresponding to the decoded  
7 subsymbol information.

1 14. The equalizer of Claim 13, wherein said demodulation unit further comprises a  
2 symbol correlator coupled to said decoding processing logic to correlate the perceived  
3 second number of chips against a subset of valid candidate symbols to obtain a best match  
4 candidate, said decoding processing logic generating the decoded subsymbol information  
5 based on the best match candidate.

1 15. The equalizer of Claim 13, wherein said demodulation unit further comprises  
2 decision processing logic capable of deciding the symbol upon receipt of the first number of  
3 chips defining the symbol.

1 16. The equalizer of Claim 15, wherein said decision processing logic comprises first  
2 and second demodulation pathways capable of deciding the symbol by at least one of first  
3 and second distinct modulation modes.

1 17. The equalizer of Claim 16, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

1 18. The equalizer of Claim 10, wherein the symbol is modulated in accordance with  
2 one of Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999).

1 19. A transceiver, comprising:  
2 a feedback equalizer capable of receiving a modulated signal, the modulated signal  
3 including a symbol defined by a first number of chips; and  
4 a subsymbol processor coupled to said feedback equalizer to generate a subsymbol  
5 waveform upon receipt of a second number of chips of the symbol and provide the  
6 subsymbol waveform to the feedback equalizer, the second number being less than the first  
7 number, said feedback equalizer to equalize the modulated signal using the subsymbol  
8 waveform.

1 20. The transceiver of Claim 19, wherein the subsymbol waveform includes a third  
2 number of chips, the third number being less than or equal to the second number.

1 21. The transceiver of Claim 19, said feedback equalizer comprising:  
2 a hard decision unit coupled to said equalizer for determining hard decision  
3 information associated with the modulated signal ; and  
4 a feedback filter coupled to said hard decision unit and said symbol processor to  
5 selectively equalize the modulated signal using one of the hard decision information and the  
6 subsymbol waveform.

1 22. The transceiver of Claim 19, wherein the symbol processor comprises:  
2 a demodulation unit coupled said feedback equalizer and comprising decoding  
3 processing logic capable of generating decoded subsymbol information upon perceiving the  
4 second number of chips of the symbol; and  
5 a remodulation unit coupled to said demodulation unit and said feedback equalizer,  
6 said remodulation unit generating a subsymbol waveform corresponding to the decoded  
7 subsymbol information.

1 23. The transceiver of Claim 22, wherein said demodulation unit further comprises a  
2 symbol correlator coupled to said decoding processing logic to correlate the perceived  
3 second number of chips against a subset of valid candidate symbols to obtain a best match  
4 candidate, said decoding processing logic generating the decoded subsymbol information  
5 based on the best match candidate.

1 24. The transceiver of Claim 22, wherein said demodulation unit further comprises  
2 decision processing logic capable of deciding the symbol upon receipt of the first number of  
3 chips defining the symbol.

1 25. The transceiver of Claim 24, wherein said decision processing logic comprises first  
2 and second demodulation pathways capable of deciding the symbol by at least one of first  
3 and second distinct modulation modes.

1 26. The transceiver of Claim 25, wherein said first and second distinct modulation  
2 modes comprise Barker spreading and complementary code keying (CCK) compliant with  
3 IEEE Standard 802.11b (1999) respectively.

1 27. The transceiver of Claim 19, wherein the symbol is modulated in accordance with  
2 one of Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999).

1 28. The transceiver of Claim 19, further comprising RF and IF sections coupled to said  
2 feedback equalizer to provide the modulated signal to said feedback equalizer.

1 29. A base station comprising the transceiver of Claim 28.

1 30. A network card comprising the transceiver of Claim 28.

1 31. An information processing system, comprising the transceiver of Claim 19.

1 32. A decoding method for a modulated signal including a symbol defined by a first  
2 number of chips, comprising:  
3 generating a subsymbol waveform upon receipt of a second number of chips of the  
4 symbol, the second number being less than the first number; and  
5 equalizing the modulated signal using the subsymbol waveform.

1 33. The method of Claim 32, wherein the subsymbol waveform includes a third number  
2 of chips, the third number being less than or equal to the second number.

1 34. The method of Claim 32, further comprising:

2 determining hard decision information associated with the modulated signal ; and  
3 wherein said equalizing step comprises selectively equalizing the modulated signal  
4 using one of the hard decision information and the subsymbol waveform.

1 35. The method of Claim 32, wherein said generating step comprises:  
2 generating decoded subsymbol information upon perceiving the second number of  
3 chips of the symbol; and  
4 generating a subsymbol waveform corresponding to the decoded subsymbol  
5 information.

1 36. The method of Claim 35, further comprising:  
2 correlating the perceived second number of chips against a subset of valid candidate  
3 symbols to obtain a best match candidate; and  
4 wherein said decoded subsymbol generating step comprises generating the decoded  
5 subsymbol information based on the best match candidate.

1 37. The method of Claim 35, further comprising deciding the symbol upon receipt of  
2 the first number of chips defining the symbol.

1 38. The method of Claim 37, wherein said deciding step comprises deciding the symbol  
2 by at least one of first and second distinct modulation modes.

1 39. The method of Claim 38, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

1 40. The method of Claim 32, wherein the symbol is modulated in accordance with one  
2 of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard  
3 802.11b (1999).

1 41. A computer program product, comprising computer readable program code causing  
2 an information processor to perform the following steps, comprising:  
3 receiving a modulated signal, the modulated signal including a symbol defined by a  
4 first number of chips;

5 generating a subsymbol waveform upon receipt of a second number of chips of the  
6 symbol, the second number being less than the first number; and  
7 equalizing the modulated signal using the subsymbol waveform.

1 42. The product of Claim 41, wherein the subsymbol waveform includes a third  
2 number of chips, the third number being less than or equal to the second number.

1 43. The product of Claim 41, further comprising:  
2 computer readable program code causing the information processor to perform the  
3 step of determining hard decision information associated with the modulated signal ; and  
4 wherein said equalizing step comprises selectively equalizing the modulated signal  
5 using one of the hard decision information and the subsymbol waveform.

1 44. The product of Claim 41, wherein said generating step comprises:  
2 generating decoded subsymbol symbol information upon perceiving the second  
3 number of chips of the symbol; and  
4 generating a subsymbol waveform corresponding to the decoded subsymbol  
5 information.

1 45. The product of Claim 44, further comprising:  
2 computer readable program code causing the information processor to perform the  
3 step of correlating the perceived second number of chips against a subset of valid candidate  
4 symbols to obtain a best match candidate; and  
5 wherein said decoded subsymbol symbol generating step comprises generating the  
6 decoded subsymbol information based on the best match candidate.

1 46. The product of Claim 44, further comprising computer readable program code  
2 causing the information processor to perform the step of deciding the symbol upon receipt  
3 of the first number of chips defining the symbol.

1 47. The product of Claim 46, wherein said deciding step comprises deciding the symbol  
2 by at least one of first and second distinct modulation modes.

1 48. The product of Claim 47, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

4 49. The product of Claim 41, wherein the symbol is modulated in accordance with one  
5 of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard  
6 802.11b (1999).

1 50. An information processing system including an information processor coupled to  
2 memory, the memory comprising computer readable program code causing the information  
3 processor to perform the following operations, comprising:

4 receiving a modulated signal, the modulated signal including a symbol defined by a  
5 first number of chips;

6 generating a subsymbol waveform upon receipt of a second number of chips of the  
7 symbol, the second number being less than the first number; and

8 equalizing the modulated signal using the subsymbol waveform.

1 51. The system of Claim 50, wherein the subsymbol waveform includes a third number  
2 of chips, the third number being less than or equal to the second number.

1 52. The system of Claim 50, wherein the memory further comprises  
2 computer readable program code causing the information processor to perform the  
3 step of determining hard decision information associated with the modulated signal ; and

4 wherein said equalizing step comprises selectively equalizing the modulated signal  
5 using one of the hard decision information and the subsymbol waveform.

1 53. The system of Claim 50, wherein said generating step comprises:  
2 generating decoded subsymbol information upon perceiving the second number of  
3 chips of the symbol; and

4 generating a subsymbol waveform corresponding to the decoded subsymbol  
5 information.

1 54. The system of Claim 53, wherein the memory further comprises



2 computer readable program code causing the information processor to perform the  
3 step of correlating the perceived second number of chips against a subset of valid candidate  
4 symbols to obtain a best match candidate; and  
5 wherein said decoded subsymbol generating step comprises generating the decoded  
6 subsymbol information based on the best match candidate.

1 55. The system of Claim 53, wherein the memory further comprises computer readable  
2 program code causing the information processor to perform the step of deciding the symbol  
3 upon receipt of the first number of chips defining the symbol.

1 56. The system of Claim 55, wherein said deciding step comprises deciding the symbol  
2 by at least one of first and second distinct modulation modes.

1 57. The system of Claim 56, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

1 58. The system of Claim 41, wherein the symbol is modulated in accordance with one  
2 of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard  
3 802.11b (1999).

1 59. A decoder, comprising:  
2 a feedback equalizer capable of receiving a modulated signal, the modulated signal  
3 including a Barker encoded symbol defined by a first number of chips; and  
4 a symbol processor coupled to said feedback equalizer to generate a decided  
5 waveform upon receipt of the first number of chips of the symbol and provide the decided  
6 waveform to the feedback equalizer, said feedback equalizer to equalize the modulated  
7 signal using the decided waveform.

1 60. The decoder of Claim 59, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.

1 61. The decoder of Claim 60, wherein  
2 the non-Barker encode symbol comprises a CCK encoded symbol; and

3 wherein the Barker encoded and CCK encoded symbols are modulated in  
4 compliance with IEEE Standard 802.11b (1999).

1 62. A transceiver, comprising the decoder of Claim 61.

1 63. A base station, comprising the transceiver of Claim 62.

1 64. A network card comprising the transceiver of Claim 62.

1 65. An information processing system comprising the transceiver of Claim 62.

1 66. A feedback equalizer comprising:

2 a summing unit having an output and first input for receiving a modulated signal,  
3 the modulated signal including a Barker encoded symbol defined by a first number of chips;

4 a symbol processor coupled to said output of said summing unit, said symbol  
5 processor capable of generating a decided waveform upon receipt of the first number of  
6 chips of the symbol; and

7 a feedback filter coupled to a second input of said summing unit and said symbol  
8 processing unit to selectively filter the decided waveform from said modulated signal.

1 67. The equalizer of Claim 66, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.

1 68. The equalizer of Claim 67, wherein

2 the non-Barker encode symbol comprises a CCK encoded symbol; and

3 wherein the Barker encoded and CCK encoded symbols are modulated in  
4 compliance with IEEE Standard 802.11b (1999).

1 69. A decoding method for a modulated signal including a Barker encoded symbol  
2 defined by a first number of chips, comprising:

3 generating a decided waveform upon receipt of the first number of chips of the  
4 symbol; and

5 equalizing the modulated signal using the decided waveform.

1 70. The method of Claim 69, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.

1 71. The method of Claim 70, wherein  
2 the non-Barker encode symbol comprises a CCK encoded symbol; and  
3 wherein the Barker encoded and CCK encoded symbols are modulated in  
4 compliance with IEEE Standard 802.11b (1999).

1 72. A computer program product, comprising computer readable program code causing  
2 an information processor to perform the following steps, comprising:  
3 receiving a modulated signal including a Barker encoded symbol defined by a first  
4 number of chips;  
5 generating a decided waveform upon receipt of the first number of chips of the  
6 symbol; and  
7 equalizing the modulated signal using the decided waveform.

1 73. The product of Claim 72, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.

1 74. The product of Claim 73, wherein  
2 the non-Barker encode symbol comprises a CCK encoded symbol; and  
3 wherein the Barker encoded and CCK encoded symbols are modulated in  
4 compliance with IEEE Standard 802.11b (1999).

1 75. An information processing system including an information processor coupled to  
2 memory, the memory comprising computer readable program code causing the information  
3 processor to perform the following operations, comprising:  
4 receiving a modulated signal including a Barker encoded symbol defined by a first  
5 number of chips;  
6 generating a decided waveform upon receipt of the first number of chips of the  
7 symbol; and  
8 equalizing the modulated signal using the decided waveform.

1 76. The system of Claim 75, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.

1 77. The system of Claim 76, wherein  
2 the non-Barker encode symbol comprises a CCK encoded symbol; and  
3 wherein the Barker encoded and CCK encoded symbols are modulated in compliance with  
4 IEEE Standard 802.11b (1999).

1 78. A decoding unit, comprising:  
2 a decision feedback equalizer having an input capable of receiving modulated signal  
3 including a received symbol defined by a first number of chips and an output;  
4 a demodulation unit coupled to the output of said decision feedback equalizer,  
5 comprising:  
6 a decoder capable of deciding the received symbol upon receipt of the first  
7 number of chips defining the received symbol; and  
8 partial correlation logic capable of generating a decoded subsymbol upon  
9 receipt of a second number of chips of the received symbol, the second number being less  
10 than the first number; and  
11 a remodulation unit coupled to said partial correlation logic of said demodulation  
12 unit and said decision feedback equalizer, said remodulation unit capable of generating a  
13 subsymbol waveform corresponding to the decoded subsymbol, said decision feedback  
14 equalizer to equalize the modulated signal using the subsymbol waveform.

1 79. The decoding unit of Claim 78, wherein the subsymbol waveform includes a third  
2 number of chips corresponding to the subsymbol waveform, the third number being less  
3 than or equal to the second number; and wherein said partial correlation logic generates the  
4 decoded subsymbol using correlation processing based on the second number of chips.

1 80. The decoding unit of Claim 78, said decision feedback equalizer comprising:  
2 a hard decision unit coupled to said equalizer input for determining hard decision  
3 information associated with the modulated signal; and

4 a feedback filter coupled to said hard decision unit and said remodulation unit for  
5 equalizing the modulated signal using one of the hard decision information and the  
6 subsymbol waveform.

1 81. The decoding unit of Claim 78, wherein said decoder of said demodulation unit  
2 comprise first and second demodulator units capable of deciding the received symbol by at  
3 least one of first and second distinct modulation modes.

1 82. The decoding unit of Claim 81, wherein said first and second distinct modulation  
2 modes comprise Barker spreading and complementary code keying compliant with IEEE  
3 Standard 802.11b (1999).

1 83. A decoder, comprising:  
2 means for receiving a modulated signal, the modulated signal including a symbol  
3 defined by a first number of chips; and  
4 means for generating a subsymbol waveform upon receipt of a second number of  
5 chips of the symbol and provide the subsymbol waveform to the receiving means, the  
6 second number being less than the first number, said receiving means including means for  
7 equalizing the modulated signal using the subsymbol waveform.

1 84. The decoder of Claim 83, wherein the subsymbol waveform includes a third  
2 number of chips, the third number being less than or equal to the second number.

1 85. The decoder of Claim 83, said equalizing means comprising:  
2 hard decision means for determining hard decision information associated with the  
3 modulated signal ; and  
4 filtering means for selectively equalizing the modulated signal using one of the hard  
5 decision information and the subsymbol waveform.

1 86. The decoder of Claim 83, wherein said generating means comprises:  
2 demodulation means for generating decoded subsymbol information upon  
3 perceiving the second number of chips of the symbol; and  
4 remodulation means for remodulating a subsymbol waveform corresponding to the  
5 decoded subsymbol information.

1 87. The decoder of Claim 86, wherein said demodulation means further comprises  
2 symbol correlator means for correlating the perceived second number of chips against a  
3 subset of valid candidate symbols to obtain a best match candidate, said demodulation  
4 means generating the decoded subsymbol information based on the best match candidate.

1 88. The decoder of Claim 86, wherein said demodulation means further comprises  
2 decision processing means for deciding the symbol upon receipt of the first number of chips  
3 defining the symbol.

1 89. The decoder of Claim 88, wherein said decision processing means comprises first  
2 and second demodulation pathway means capable of deciding the symbol by at least one of  
3 first and second distinct modulation modes.

1 90. The decoder of Claim 89, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

1 91. The decoder of Claim 83, wherein the symbol is modulated in accordance with one  
2 of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard  
3 802.11b (1999).

1 92. A feedback equalizer comprising:  
2 means for receiving a modulated signal, the modulated signal including a symbol  
3 defined by a first number of chips;  
4 means for generating a subsymbol waveform upon receipt of a second number of  
5 chips of the symbol, the second number being less than the first number; and  
6 means for selectively filtering the subsymbol waveform from said modulated signal.

1 93. The equalizer of Claim 92, wherein the subsymbol waveform includes a third  
2 number of chips, the third number being less than or equal to the second number

1 94. The equalizer of Claim 92, further comprising:  
2 means for determining hard decision information associated with the modulated  
3 signal ; and

4 means for selectively equalizing the modulated signal using one of the hard decision  
5 information and the subsymbol waveform.

1 95. The equalizer of Claim 92, wherein said generating means comprises:  
2 demodulation means for generating decoded subsymbol information upon  
3 perceiving the second number of chips of the symbol; and  
4 remodulation means for generating a subsymbol waveform corresponding to the  
5 decoded subsymbol information.

1 96. The equalizer of Claim 95, wherein said demodulation means further comprises  
2 means for correlating the perceived second number of chips against a subset of valid  
3 candidate symbols to obtain a best match candidate, said demodulation means generating  
4 the decoded subsymbol information based on the best match candidate.

1 97. The equalizer of Claim 95, wherein said demodulation means further comprises  
2 decision processing means for deciding the symbol upon receipt of the first number of chips  
3 defining the symbol.

1 98. The equalizer of Claim 97, wherein said decision processing means comprises first  
2 and second demodulation pathway means for deciding the symbol by at least one of first  
3 and second distinct modulation modes.

1 99. The equalizer of Claim 98, wherein said first and second distinct modulation modes  
2 comprise Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999) respectively.

1 100. The equalizer of Claim 91, wherein the symbol is modulated in accordance with one  
2 of Barker spreading and complementary code keying (CCK) compliant with IEEE Standard  
3 802.11b (1999).

1 101. A transceiver, comprising:  
2 means for receiving a modulated signal, the modulated signal including a symbol  
3 defined by a first number of chips; and

4 means for generating a subsymbol waveform upon receipt of a second number of  
5 chips of the symbol and provide the subsymbol waveform to the receiving means, the  
6 second number being less than the first number, said receiving means including means for  
7 equalizing the modulated signal using the subsymbol waveform.

1 102. The transceiver of Claim 101, wherein the subsymbol waveform includes a third  
2 number of chips, the third number being less than or equal to the second number.

1 103. The transceiver of Claim 101, said equalizing means comprising:

2 hard decision means for determining hard decision information associated with the  
3 modulated signal ; and

4 filtering means for selectively equalizing the modulated signal using one of the hard  
5 decision information and the subsymbol waveform.

1 104. The transceiver of Claim 101, wherein said generating means comprises:

2 demodulation means for generating decoded subsymbol information upon  
3 perceiving the second number of chips of the symbol; and

4 remodulation means for re-modulating a subsymbol waveform corresponding to the  
5 decoded subsymbol information.

1 105. The transceiver of Claim 104, wherein said demodulation means further comprises

2 symbol correlator means for correlating the perceived second number of chips against a  
3 subset of valid candidate symbols to obtain a best match candidate, said demodulation

4 means generating the decoded subsymbol information based on the best match candidate.

1 106. The transceiver of Claim 104, wherein said demodulation means further comprises

2 decision processing means for deciding the symbol upon receipt of the first number of chips  
3 defining the symbol.

1 107. The transceiver of Claim 106, wherein said decision processing means comprises

2 first and second demodulation pathway means capable of deciding the symbol by at least  
3 one of first and second distinct modulation modes.



- 1 108. The transceiver of Claim 107, wherein said first and second distinct modulation  
2 modes comprise Barker spreading and complementary code keying (CCK) compliant with  
3 IEEE Standard 802.11b (1999) respectively.
- 1 109. The transceiver of Claim 101, wherein the symbol is modulated in accordance with  
2 one of Barker spreading and complementary code keying (CCK) compliant with IEEE  
3 Standard 802.11b (1999).19.
- 1 110. The transceiver of Claim 101, further comprising RF and IF means for providing  
2 the modulated signal to said receiving means.
- 1 111. A base station comprising the transceiver of Claim 110.
- 1 112. A network card comprising the transceiver of Claim 110.
- 1 113. An information processing system, comprising the transceiver of Claim 101.
- 1 114. A decoder, comprising:  
2 means for receiving a modulated signal, the modulated signal including a Barker  
3 encoded symbol defined by a first number of chips; and  
4 means for generating a decided waveform upon receipt of the first number of chips  
5 of the symbol and provide the decided waveform to the receiving means, said receiving  
6 means including means for equalizing the modulated signal using the decided waveform.
- 1 115. The decoder of Claim 114, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.
- 1 116. The decoder of Claim 115, wherein  
2 the non-Barker encode symbol comprises a CCK encoded symbol; and  
3 wherein the Barker encoded and CCK encoded symbols are modulated in  
4 compliance with IEEE Standard 802.11b (1999).
- 1 117. A transceiver, comprising the decoder of Claim 116.
- 1 118. A base station, comprising the transceiver of Claim 117.

- 1 119. A network card comprising the transceiver of Claim 117.
- 1 120. An information processing system comprising the transceiver of Claim 117.
- 1 121. A feedback equalizer comprising:  
2 means for receiving a modulated signal, the modulated signal including a Barker  
3 encoded symbol defined by a first number of chips;  
4 means for generating a decided waveform upon receipt of the first number of chips  
5 of the symbol; and  
6 means for selectively filtering the decided waveform from said modulated signal.
- 1 122. The equalizer of Claim 121, wherein the modulated signal further includes a non-  
2 Barker encoded symbol defined by a second number of chips.
- 1 123. The equalizer of Claim 122, wherein  
2 the non-Barker encode symbol comprises a CCK encoded symbol; and  
3 wherein the Barker encoded and CCK encoded symbols are modulated in compliance with  
4 IEEE Standard 802.11b (1999).
- 1 124. A decoding unit, comprising:  
2 decision feedback equalization means having an input capable of receiving  
3 modulated signal including a received symbol defined by a first number of chips and an  
4 output;  
5 demodulation means comprising:  
6 decoding means for deciding the received symbol upon receipt of the first  
7 number of chips defining the received symbol; and  
8 partial correlation logic means for generating a decoded subsymbol upon  
9 receipt of a second number of chips of the received symbol, the second number being less  
10 than the first number; and  
11 remodulation means for generating a subsymbol waveform corresponding to the  
12 decoded subsymbol, said decision feedback equalization means including means for  
13 equalizing the modulated signal using the subsymbol waveform.

1 125. The decoding unit of Claim 124, wherein the subsymbol waveform includes a third  
2 number of chips corresponding to the subsymbol waveform, the third number being less  
3 than or equal to the second number; and wherein said partial correlation logic means  
4 generates the decoded subsymbol using correlation processing based on the second number  
5 of chips.

1 126. The decoding unit of Claim 124, said decision feedback equalization means  
2 comprising:  
3 hard decision means for determining hard decision information associated with the  
4 modulated signal ; and  
5 feedback filter means for equalizing the modulated signal using one of the hard  
6 decision information and the subsymbol waveform.

1 127. The decoding unit of Claim 124, wherein said decoding means comprises first and  
2 second demodulator means for deciding the received symbol by at least one of first and  
3 second distinct modulation modes.

1 128. The decoding unit of Claim 127, wherein said first and second distinct modulation  
2 modes comprise Barker spreading and complementary code keying compliant with IEEE  
3 Standard 802.11b (1999).

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